Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **N. 1E**
2. **S1**
3. **1I3**
4. **1I2**
5. **1I1**
6. **1I0**
7. **1Y**
8. **GND**
9. **2Y**
10. **2I0**
11. **2I1**
12. **2I2**
13. **2I3**
14. **SO**
15. **N.2E**
16. **VCC**

**.070”**

**.088”**

**6 5 4 3**

**2**

**1**

**16**

**15**

**7**

**8**

**9**

**10 11 12 13 14**

**MASK**

**REF**

**HC153**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size = .004 x .004”**

**Backside Potential: VCC**

**Mask Ref: HC153**

**APPROVED BY: DK DIE SIZE .070” X .088” DATE: 7/11/22**

**MFG: TEXAS INSTRUMENTS THICKNESS .010” P/N: 54HC153**

**DG 10.1.2**

#### Rev B, 7/1